REMARKS/ARGUMENTS

Favorable reconsideration of this application, in view of the present amendment and in light of the following discussion, is respectfully requested.

Claims 1-13 are pending in this application. Claims 1, 2, 6, 7, and 11-13 are amended, and support for the amendments is found in the Applicants' specification at least at page 40, line 17 to page 42, line 13 and Figure 9. Claims 3-5, 8-10, 12, and 13 are withdrawn from consideration. It is respectfully submitted that no new matter is added by this amendment.

In the outstanding Office Action, the Title was objected to as not descriptive; Claims 1, 2, 6 and 7 were rejected under 35 U.S.C. § 112, second paragraph, as indefinite; Claim 11 was rejected under 35 U.S.C. § 102(b) as anticipated by Okino (U.S. Patent No. 5,754,705); and Claims 1, 2, 6, and 7 were rejected under 35 U.S.C. § 103(a) as unpatentable over Okino.

Applicants and Applicants' representatives thank Examiner Poon for the interview granted Applicants' representatives on May 18, 2005. During the interview, the claimed invention and how the claimed invention differs from the cited reference of Okino was explained with respect to independent Claim 1. More specifically, Applicants' representatives discussed that Okino fails to disclose, teach, or suggest "a switch configured to divide image data into m x n pixels, having n lines with m pixels per one line and to transfer without storing in the switch each one of the n lines of image data to a predetermined destination." No agreement was reached, subject to the Examiner's detailed reconsideration of the application upon formal submission of a response.

In response to the objection to the Title, the Title is amended to recite "IMAGE PROCESSOR INCLUDING A DATA COMPRESSION UNIT HAVING A SWITCH AND IMAGE PROCESSING METHOD THEREOF." Therefore, Applicants respectfully request that the objection to the Title be withdrawn.

In response to the rejection of Claims 1, 2, 6, and 7 under 35 U.S.C. § 112, second paragraph, as indefinite, Claims 1, 2, 6, and 7 are amended to clarify the features of the claims, thereby obviating the rejection. Accordingly, Applicants respectfully request that the rejection of Claims 1, 2, 6, and 7 under 35 U.S.C. § 112, second paragraph, be withdrawn.

Previously withdrawn method Claims 12 and 13 are amended to delete "the steps of" and "step" language from the claims.

Before turning to the outstanding art rejections, it is believed that a brief review of the claimed invention is useful. Amended Claim 1 recites an image processor including "a switch configured to divide image data into m x n pixels, having n lines with m pixels per one line and to **transfer without storing in the switch** each one of the n lines of image data to a predetermined destination;" a storage unit "including (n-1) number of memories each configured to store one line of the n lines of the image data;" a control unit configured to control the transfer of each one of the n lines of the image data; and a compression unit configured to batch compress the image data of m x n pixels. The control unit is further configured "to control said switch to **directly transfer** (n-1) lines of the n lines of the image data to the (n-1) number of memories, and a remaining one line of the n lines of the image data directly to said compression unit; and to control the storage unit to transfer the (n-1) lines of the image data stored in the (n-1) number of memories to said compression unit." Independent Claim 6 is amended to invoke a means-plus-function interpretation under 35 U.S.C. § 112, sixth paragraph, and recites features similar to the features discussed above with respect to amended independent Claim 1. Further, amended Claim 11 recites an image processing method including dividing image data into m x n pixels; "**transferring without storing** each one of the n lines of the image data to predetermined destination; switching the predetermined destination for each one of the n line of the image data; storing one line of the n lines of the image data in each of (n-1) number of memories;" and batch compressing the

image data of m x n pixels. Further, the transferring step recited in amended Claim 11 "**directly transfers** (n-1) lines of the n lines of the image data to said (n-1) number of memories and the remaining one line of the n lines of the image data directly to a compression unit based on said switching; and transfers the (n-1) lines stored in the (n-1) number of memories to said compression unit."

As described in a non-limiting example in Applicants' specification on page 40, line 17 to page 43, line 3, image data is directly transferred through switch 903 to either the FIFO memories FM1, FM2, FM3, or the compression device 902. The switch recited in amended Claims 1 and 6 and the switching in amended Claim 11 determines the predetermined destination where the image data is transferred.

In regard to the rejection of Claim 11 under 35 U.S.C. § 102(b) as anticipated by Okino, Applicants respectfully traverse the rejection for the following reasons.

Okino is directed to a two-dimensional image sensor for reading an image of an object, and to an image processing method for performing digital processing on two-dimensional object information obtained by sub-scanning the image sensor.[1] The background section of Okino describes a conventional image processing method referencing Figures 2a and 2b. As shown in Figures 2a and 2b, the first row of signal charges including n pixels is loaded into a horizontal shift register 303, and supplied through an amplifier 304 to an A/D converter 305, where the pixels are digitized.[2] When all the signals of the n pixels in the first row are output by the shift register, the signals of a second row are transferred into the horizontal shift register 303.[3] After the horizontal shift register 303 transfers the rows of pixels to the amplifier 304 and the A/D converter 305, the rows of pixels are transferred and stored in buffer memory 306. As shown in Figure 2a, the buffer memory 306 stores seven

[1] Okino, column 1, lines 11-15.
[2] Okino, column 2, lines 59-67.
[3] Okino, column 3, lines 1-5.

rows of pixels that are later transferred to the compression processor 307. Further, when the signals of an eighth row are output from shift register 303, the pixels of the eighth row are transferred via the amplifier 304 and A/D converter 305 to a compression processor 307.

As described above, in Okino, the shift register 303 acts as an interim storage for each row of pixels. Therefore, Okino does not disclose "transferring **without storing** each one of the n lines of the image data to a predetermined destination; switching the predetermined destination for the each one of the n lines of the image data;" wherein said transferring "**directly transfers** (n-1) lines of the n lines of the image data to said (n-1) number of memories and the remaining one line of the n lines of the image data directly to a compression unit based on said switching; and transfers the (n-1) line stored in the (n-1) number of memories to said compression unit."

Accordingly, Okino does not disclose, teach, or suggest each feature of amended independent Claim 11. Therefore, Applicants respectfully request that the rejection of Claim 11 under 35 U.S.C. § 102(b) be withdrawn.

In regard to the rejections of Claims 1, 2, 6, and 7 under 35 U.S.C. § 103(a) as unpatentable over Okino, Applicants respectfully traverse the rejection for the following reasons.

As described above, Okino discloses a shift register 303 used to store and transfer each row of pixels through an amplifier 304 and a A/D converter to a buffer memory 306. Then, the data stored in the buffer memory 306 is transferred to the compression processor 307, and the final row of pixels stored in the shift register 303 is transferred through the amplifier 304 and the A/D converter 305 to the compression processor 307.

Therefore, Okino does not disclose, teach, or suggest "a switch configured to divide image data into m x n pixels, having n lines with m pixels per one line and to **transfer without storing in the switch** each one of the n lines of image data to a predetermined

destination." Since Okino does not disclose a switch, Okino also fails to disclose, teach, or suggest a control unit "configured to control said switch to **directly transfer** (n-1) lines of the n lines of the image data to the (n-1) number of memories, and a remaining one line of the m lines of the image data directly to said compression unit; and to control the storage unit to transfer the (n-1) lines of the image data stored in the (n-1) number of memories to said compression unit," as recited in amended independent Claim 1.

Likewise, Okino also fail to disclose, teach, or suggest each and every feature of amended independent Claim 6 that recites features similar to the above-identified features of amended independent Claim 1.

Accordingly, Applicants respectfully request that the rejection of independent Claims 1 and 6 under 35 U.S.C. § 103(a) be withdrawn.

Claims 2 and 7 depend from independent Claims 1 and 6, respectively, and therefore Claims 2 and 7 also recite the above-identified patentably distinguishing features of amended independent Claims 1 and 6.

Therefore, Applicants also respectfully request that the rejection of dependent Claims 2 and 7 under 35 U.S.C. § 103(a) be withdrawn.

Consequently, in view of the present amendment and in light of the above discussion, it is respectfully submitted that the present application is in condition for formal allowance, and an early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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